Call: H2020-ICT-2014-2
Project reference: 671660

Project Name:
Flexible Air iNTerfAce for Scalable service delivery wiThin wIreless Communication networks of the 5th Generation (FANTASTIC-5G)

Deliverable D5.1
Identification of the PoC scenarios

Date of delivery: 30/05/2016
Start date of project: 01/07/2015
Version: 1.0
Duration: 24 months
Abstract

The proof-of-concepts (PoC) in FANTASTIC-5G target to implement key technical components developed within the project. The demonstration aims at validating the feasibility and the superiority of the different components of the foreseen 5G air interface.

For this activity, several platforms are being developed in FANTASTIC-5G. The planned demonstrations are categorized into three main categories: post-orthogonal frequency division multiplexing (OFDM) waveform prototyping, coexistence aspects evaluation and broadcast and multicast software defined radio-based PoC.

This deliverable aims at identifying PoC scenarios envisaged in the project. As a consequence, it will provide the necessary information on the approved scenarios and selected techniques. Additionally, it provides a description of the available/to be developed software and hardware platforms.

Keywords

5G, proof-of-concept, post-OFDM, waveform, KPI, scenarios, vehicular communications, massive machine communications, mission critical communications, hardware complexity, error rate, latency, power consumption, transceiver algorithm, FBMC, FC-ODM, CP-OFDM, UF-OFDM, software programmable hardware, software defined radio, MIMO, P-OFDM, hardware-in-the-loop, broadcast and multicast.
Executive Summary

The proof-of-concepts (PoC) in FANTASTIC-5G target to implement key technical components developed within the project. The demonstration aims at validating the feasibility and the superiority of the different components of the foreseen 5G air interface.

This document intends to provide the necessary information on the approved scenarios and selected techniques. Additionally, it provides a description of the available/to be developed software and hardware platforms.

The planned PoCs in FANTASTIC-5G are classified into three main categories: post-orthogonal frequency division multiplexing (OFDM) waveform prototyping, coexistence aspects evaluation and software defined radio (SDR) - based demonstration for enhanced broadcast and multicast transmission.

Taking into account that post-OFDM waveforms are foreseen as key enablers to several 5G scenarios as they enhance system robustness to different types of impairments, the post-OFDM prototyping addresses the building of PoCs for the algorithms developed in FANTASTIC-5G to tackle open issues like synchronization, channel estimation, equalization, efficient multi-input multi-output (MIMO) support and pulse shape adaptation.

To that end, the development of Filter Bank Multi-Carrier (FBMC), Flexible Configured (FC)-OFDM, and Universal-Filtered (UF)-OFDM transceivers is intended from algorithm simplification and optimization to on-board validation and demonstration. The transceivers will be tested in both vehicular, massive machine communications (MMC) and Mission critical communication (MCC) scenarios. The different key performance indicators (KPIs) are specified to include power consumption, hardware complexity, error rate, power leakage, throughput, latency and robustness against Doppler and synchronization errors. Additionally, flexible 2x2 MIMO-FBMC based transceiver based on software programmable hardware is considered with the objective of conducting a trade-off analysis of complexity vs. impairments robustness vs. throughput. The main focus is on relaxed synchronization and channel estimation in multi-antenna case. The applied scenarios are related to MBB core service and 50Mbps everywhere use case. Furthermore, Pulse shaped OFDM (P-OFDM) for timing adjustment (TA)-free low latency transmission demonstrator is targeted where a hardware-in-the-loop platform will be adopted for the performance evaluation. The P-OFDM demonstration main focus is on two different scenarios; the asynchronous uplink transmission for MMC scenario in addition to high mobility vehicular communication scenario. The KPIs to be considered include reliability in terms of packet error rate (PER) and bit error rate (BER), robustness in high Doppler scenarios, complexity and latency aspects. Last but not least, a modified waveform for MCC scenarios will be implemented with the focus on low latency transmission under reliability constraints as defined by the MCC services in the factory automation scenario. The KPIs to be evaluated include latency percentiles, latency jitter, and reliability targets under given data rate demands.

The basic idea of the coexistence aspects evaluation is focusing on the implementation of different waveforms like 4G’s Cyclic Prefix (CP)-OFDM, as well as modified FBMC and filtered CP-OFDM waveforms in dense networks in order to evaluate signal to interference noise ratio (SINR), resulting data rates, interference power as in the adjacent channel leakage power ratio (ACLR), and carrier frequency offsets (CFO) when comparing orthogonal and non-orthogonal waveforms.

Eventually, an efficient and reliable integration of broadcast and multicast services with mobile broadband wireless networks will benefit an efficient provision of multiple services in 5G systems. Techniques are being developed within FANTASTIC-5G to efficiently exploit the use of MIMO and non-orthogonal transmission as well as advanced protocol solutions [FAN16-D4.1]. In particular, the advanced techniques that are being developed in FANTASTIC-5G to
enable multicast transmissions to different multicast groups by the use of MIMO techniques but, at the same time, provide a common broadcast layer to all users will be demonstrated using software defined radio (SDR) platform. The KPIs to be evaluated include PER, BER, SNR at the user equipment (UE) and aggregated throughput of the cell.
Table of Contents

List of Figures ............................................................................................................. 7
List of Tables .................................................................................................................. 8
List of Acronyms and Abbreviations .......................................................... 9

1 Introduction .............................................................................................................. 11
  1.1 Objective of the document ................................................................................. 11
  1.2 Structure of the document ................................................................................. 11

2 Post-OFDM waveform prototyping PoC ................................................................. 12
  2.1 Flexible PoC for Post-OFDM waveforms ......................................................... 12
  2.1.1 Scenarios, use cases, system parameters and KPI ...................................... 12
  2.1.2 FBMC transceiver algorithm and control functionality ............................... 14
  2.1.3 FC-OFDM transceiver algorithm and control functionality .................... 17
  2.1.4 UF-OFDM transceiver algorithm and control functionality .................... 21
  2.1.5 Platform description ...................................................................................... 22
  2.2 FBMC-MIMO transceiver based on software programmable hardware .......... 25
  2.2.1 Scenarios, use cases, system parameters and KPI ...................................... 25
  2.2.2 PHY and MAC layer transceiver algorithm and control functionality ........ 27
  2.2.2.1 Architecture overview for the transmitter ............................................ 27
  2.2.2.2 Architecture overview for the receiver ................................................. 28
  2.2.3 Platform description ...................................................................................... 30
  2.2.3.1 Architecture of CEA-Leti’s main board .............................................. 31
  2.2.3.2 HSMC daughter board .......................................................................... 33
  2.3 Pulse shaped OFDM for timing adjustment (TA)-free low latency transmission .. 35
  2.3.1 Scenarios, use cases, system parameters and KPI ...................................... 35
  2.3.2 PHY and MAC layer transceiver algorithm and control functionality ........ 35
  2.3.2.1 Pulse shape design ............................................................................. 35
  2.3.2.2 Transceiver structure .......................................................................... 36
  2.3.3 Platform description ...................................................................................... 37
  2.4 Post- and Parameterized-OFDM Waveforms for Low Latency Transmission ..... 38
  2.4.1 Scenarios, use cases, system parameters and KPI ...................................... 38
  2.4.2 PHY and MAC layer transceiver algorithm and control functionality ........ 38
  2.4.3 Platform description ...................................................................................... 39

3 Coexistence aspects evaluation PoC ................................................................. 41
  3.1 Scenario, use case, system parameters and KPI .............................................. 41
  3.2 PHY and MAC layer transceiver algorithm and control functionality .......... 44
  3.3 Platform description ......................................................................................... 44

4 Broadcast and multicast SDR-based PoC .............................................................. 46
  4.1 Scenario, use case, system parameters and KPI .............................................. 46
  4.2 PHY and MAC layer transceiver algorithm and control functionality .......... 48
  4.3 Platform description ......................................................................................... 48

5 Conclusions ............................................................................................................ 50

6 References ............................................................................................................ 51

Appendix A .................................................................................................................. 53
  A.1 AD9361 architecture ......................................................................................... 53
  A.2 AD9361 Transmitter ......................................................................................... 54
  A.3 AD9361 Receiver .............................................................................................. 54
List of Figures

Figure 2-1: Flexible PoC for Post-OFDM waveforms. 12
Figure 2-2: CP-OFDM and FBMC/OQAM system description. 16
Figure 2-3: FC-OFDM transmitter architecture based on 2 IFFT. 20
Figure 2-4: Post-IFFT processing at even and odd symbol index. 20
Figure 2-5: Principle of UF-OFDM frequency domain signal approximation, illustrating generation of one subband $i$ with $NOS = 2$. 22
Figure 2-6: Development framework of the flexible PoC for Post-OFDM waveforms. 24
Figure 2-7: overall architecture of the transceiver. 26
Figure 2-8: Envisaged scenario for MIMO FBMC PoC 26
Figure 2-9: Simplified block diagram of the proposed DL Tx 28
Figure 2-10: Simplified block diagram of the proposed DL Rx 29
Figure 2-11: Simplified block diagram of the DL Physical channel processing 30
Figure 2-12: CEA-Leti’s main board architecture. 32
Figure 2-13: CEA-Leti’s main board routing and PCB. 32
Figure 2-14: Board components and dimensions. 33
Figure 2-15: Box for digital and radio boards. 33
Figure 2-16: ARRADIO board top and bottom views. 34
Figure 2-17: CEA-Leti’s HW platform, top and bottom views. 34
Figure 2-18: Pulse shapes considered. 36
Figure 2-19: Asynchronous transceiver based on P-OFDM. 36
Figure 2-20: Hardware in the loop platform based on USRP. 37
Figure 2-21: Typical 3 users and 1 BS setup. 38
Figure 2-22 HHI’s SDR toolkit based on MicroTCA form factor: The key components are radio-heads with support for 2-8 transceiver chains. 40
Figure 3-1 Multicarrier transmission chain 41
Figure 3-2 Integration of multicarrier modulator into HWIL testbed 43
Figure 3-3 Coexistence Evaluation with HHI’s SDR Toolkit 45
Figure A-1: AD9361 architecture. 53
List of Tables

Table 2-1: Characteristics of the three FC-OFDM configuration modes.......................... 19
Table 2-2: Used CP-OFDM and modified CP-OFDM parameter sets for the URLLC use case.39
Table 3-1: Parameters for multi-carrier modulator ................................................................. 44
Table 4-1: USRP X300 specifications. ........................................................................................ 49
# List of Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Abbreviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>4G</td>
<td>Fourth Generation</td>
</tr>
<tr>
<td>5G</td>
<td>Fifth Generation</td>
</tr>
<tr>
<td>ACLR</td>
<td>Adjacent Channel Leakage Power Ratio</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>ARM</td>
<td>Advanced RISC Machines</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-Specific Integrated Circuit</td>
</tr>
<tr>
<td>BBP</td>
<td>BaseBand Processor</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>BGAN</td>
<td>Broadband Global Access Network</td>
</tr>
<tr>
<td>BS</td>
<td>Base station</td>
</tr>
<tr>
<td>CASTLE</td>
<td>Cloud Architecture for Standardization Development</td>
</tr>
<tr>
<td>CFO</td>
<td>carrier frequency offset</td>
</tr>
<tr>
<td>CP</td>
<td>Cyclic-Prefix</td>
</tr>
<tr>
<td>CP-OFDM</td>
<td>Cyclic Prefix Orthogonal Frequency Division Multiplexing</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>EC</td>
<td>European Commission</td>
</tr>
<tr>
<td>FBMC</td>
<td>Filter Bank Multi-Carrier</td>
</tr>
<tr>
<td>FBMC-QAM</td>
<td>Filter Bank Multi-Carrier-Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>FC-OFDM</td>
<td>Flexible Configured - Orthogonal Frequency Division Multiplexing</td>
</tr>
<tr>
<td>FDD</td>
<td>Frequency Division Duplex</td>
</tr>
<tr>
<td>FDMA</td>
<td>Frequency Division Multiple Access</td>
</tr>
<tr>
<td>FEC</td>
<td>Forward Error Correction</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field-Programmable Gate Array</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphical User Interface</td>
</tr>
<tr>
<td>H2020</td>
<td>Horizon 2020</td>
</tr>
<tr>
<td>HARQ</td>
<td>Hybrid Automatic Repeat Request</td>
</tr>
<tr>
<td>HWIL</td>
<td>HardWare-In-the-Loop</td>
</tr>
<tr>
<td>ICT</td>
<td>Information and Communication Technologies</td>
</tr>
<tr>
<td>IFFT</td>
<td>Inverse Fast Fourier Transform</td>
</tr>
<tr>
<td>IOTA</td>
<td>Isotropic Orthogonal Transform Algorithm</td>
</tr>
<tr>
<td>KPI</td>
<td>Key Performance Indicator</td>
</tr>
<tr>
<td>LLR</td>
<td>Log-Likelihood Ratios</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LTE</td>
<td>Long Time Evolution</td>
</tr>
<tr>
<td>LTE-A</td>
<td>Long Time Evolution - Advanced</td>
</tr>
<tr>
<td>MBB</td>
<td>Mobile BroadBand</td>
</tr>
<tr>
<td>MCC</td>
<td>Mission critical communication</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multiple Input Multiple Output</td>
</tr>
<tr>
<td>ML</td>
<td>Maximum Likelihood</td>
</tr>
</tbody>
</table>
MMB  Martin-Mirabassi-Bellanger
MMC  Massive Machine Communication
OF   Overlapping Factor
OFDM Orthogonal Frequency Division Multiplexing
OOBPL Out-Of-Band Power Leakage
OQAM Offset Quadrature Amplitude Modulation
PA   Power Amplifier
PAM  Pulse-amplitude modulation
PAPR Peak to Average Power Ratio
PER  Packet Error Rate
PLL  Phase Locked Loop
PoC  Proof of Concept
P-OFDM Pulse shaped Orthogonal Frequency Division Multiplexing
PPN  PolyPhase Network
PRB  Physical Resource Block
QAM  Quadrature Amplitude Modulation
QoS  Quality of Service
QPSK Quadrature Phase Shift Keying
RF   radio frequency
RI   Roll-off Interval
RRU  Remote Radio Unit
SDR  Software Defined Radio
SDMA Space Division Multiple Access
SFBC Space Frequency Block Code
SNR  Signal-to-Noise Ratio
SoC  System on Chip
TA   Timing Adjustment
TDD  Time Division Duplexing
TFL  Time Frequency Localization
TTI  Time Transmission Interval
UE   User Equipment
UF-OFDM Universal-Filtered Orthogonal Frequency Division Multiplexing
URLLC Ultra-Reliable Low Latency Communication
USRPs Universal Software Radio Peripheral
V2X  Vehicular to anything
VCO  Voltage-Controlled Oscillator
VLC  Visible Light Communications
WP   Work-package
# 1 Introduction

## 1.1 Objective of the document

A wide range of developed techniques in the FANTASTIC-5G project will be demonstrated to validate the feasibility of these techniques and compare them with the state of the art to illustrate the unique features of FANTASTIC-5G solutions.

Considering the planned proof-of-concepts (PoC) in FANTASTIC-5G, this deliverable targets providing the following information:

- **Approved scenarios:** including the specification of the considered use-cases as well as the system parameters and the targeted KPIs based on the ones already specified in [FAN15-IR21].
- **Selected techniques:** which focuses on the specification of the technique to be adopted. In case a technique is currently developed within FANTASTIC-5G, the corresponding work package and task are specified. In particular, techniques that will be applied based on the theoretical research carried out in WP3 and WP4 will be highlighted.
- **Platform description:** which provides a description of per-partner available/to be developed software and hardware platforms.

## 1.2 Structure of the document

The rest of the document is organized in four sections,

Section 2 targets the description of the post-orthogonal frequency division multiplexing (OFDM) waveform prototyping PoC where Section 2.1 considers the flexible PoC for filter bank multi-carrier offset quadrature amplitude modulation (FBMC-OQAM), Flexible Configured (FC)-FBMC and Universal-Filtered (UF)-FBMC transceivers. Section 2.2 addresses the multiple-input multiple-output MIMO-FBMC transceiver based on software programmable hardware while Section 2.3 explains the pulse shaped OFDM for timing adjustment (TA)-free low latency transmission. Section 2.4 focuses on the PoC related to post- and parameterized-OFDM waveforms for low latency transmission.

The information related to the PoC of the coexistence aspects evaluation (co-existence between waveforms in adjacent bands) is described in Section 3 while the broadcast and multicast software defined radio-based PoC is described in Section 4. Finally, Section 5 concludes this report.
2 Post-OFDM waveform prototyping PoC

2.1 Flexible PoC for Post-OFDM waveforms

2.1.1 Scenarios, use cases, system parameters and KPI

Post-OFDM waveforms are foreseen as key enablers to several 5G scenarios as they enhance system robustness to different types of impairments [FAN16-D31]. Telecom Bretagne intends to develop a flexible PoC for post-OFDM waveforms. Jointly with Orange and NOK, three candidate waveforms will be implemented and integrated in Telecom Bretagne’s hardware platform: FBMC, FC-OFDM, and UF-OFDM.

The target PoC environment is illustrated in Figure 2-1 where one board emulates a user equipment (UE) physical layer (transmitter side), and a second board is used to emulate the base station (receiver side). Both boards are extended by an RF interface to enable on-air transmission. The TX and RX of different waveforms are implemented on the Field-Programmable Gate Array (FPGA) part of the Zynq-7000 SoC. The control and interface are ensured by a dual-core Advanced RISC Machines (ARM) cortex A9 processor embedded in the Zynq SoC and through the development of a dedicated Graphical User Interface (GUI). Details about the characteristics of the boards and the development framework are provided at the end of this section.

![Figure 2-1: Flexible PoC for Post-OFDM waveforms.](image)

The target PoC will consider at least the following scenarios.

**Vehicular communications**

This scenario corresponds to the establishment of communication links in mobile environments such as between the classical infrastructure and a moving vehicle, or communication between vehicles (V2X). Indeed, impairments appear in a situation where users are subject to high Doppler, for instance in a high speed vehicle, or in a train. The purpose is to illustrate the robustness of post-OFDM waveforms against Doppler shift compared to cyclic prefix orthogonal frequency division multiplexing (CP-OFDM). The PoC will describe a situation where a user in a high speed vehicle uploads an image or a streaming video to the base-station (uplink communication).

The effect of high mobility is emulated in the demonstrator directly in hardware through a dedicated real-time channel emulator implementing the approach proposed in [YNL13]. This approach consists of using an overlap-save method (based on FFTs) to generate in real time and
at low memory cost the channel coefficients (Rayleigh sequences correlated with Doppler). A dedicated FPGA will be used to implement this channel emulator. The extent of the mobility effect will be defined at a later stage depending on the demonstration and system-level requirements specified in WP2. The GUI at the transmitter side is used to select mapping and modulation parameters like the quadrature amplitude modulation (QAM) constellation order, the Fast Fourier Transform (FFT) and the cyclic prefix (CP) sizes, the number of active subcarriers, etc. The GUI at the receiver side displays relevant key performance indicators (KPIs).

Massive machine communications
In a dense network, cellular users may coexist with Massive machine communications (MMC)-type users such as sensors; for example by sharing the same spectrum resources. Under power and signaling overhead constraints, perfect synchronization may not be easily ensured. Therefore, interference is created between subcarriers allocated to different services or even allocated to the same type of services but to different UEs or sensors. The key aspect of this PoC scenario is to assess the behavior of post-OFDM waveforms and state-of-the-art CP-OFDM in the context of asynchronous links foreseen in MMC. The target PoC setup emulates a situation where a massive number of sensors send short packets of information to the base station. To avoid close-loop synchronization and lower the power consumption of the sensors, relaxed synchronization communication is considered in this demonstration. The sensors do not require an accurate knowledge of the time base of the base station. They wake up from sleep mode and transmit information to the base station using the pre-allocated subbands without applying any TA-procedure. In this context, sensors send small-size image files to the base station for simulating the transmission of a few bits of information at low data rate. These sensors are allocated on different subcarriers and experience different levels of synchronization misalignment with respect to the existing, already occupied, fragmented spectrum. The fragmented spectrum can be the result of the transmissions of other sensors or broadband users. Due to this lack of synchronization, the fragmented spectrum acts as interference for the considered sensors. A configurable guard-band is inserted around the subcarriers allocated to the considered sensors. Several levels of interference can be illustrated by controlling the timing offset. The flexible platform illustrated in Figure 2-1 will be used for this scenario with suited GUI at the transmitter side to select system parameters like QAM constellation order, number of subcarriers in the guard-band, number of active subcarriers, etc. The GUI at the receiver side displays relevant KPIs. At the receiver side (base station), the available antenna of the RF board is used to emulate massive traffic from interfering sensors in the case of MMC uplink scenario.

Mission critical communications
In mission critical communication (MCC) related scenarios, sensor and control messages need to be transmitted between communicating elements with very low latency and very high reliability. Typical use cases of MCC are safety and security applications (e.g. video surveillance, intrusion detection), vital sign monitoring, factory automation, etc. The high reliability requirement needs appropriate techniques such as conservative link adaptation, hybrid automatic repeat request (HARQ) and diversity sources (e.g. multiple antennas). On the other hand, post-OFDM waveforms can allow reaching the very low latency requirement by reducing the Time Transmission Interval (TTI) compared to long time evolution (LTE). TTI can be reduced by decreasing the symbol duration of the candidate waveform, which is equivalent to increasing the subcarrier spacing. However, using multiple services with different numerology in the same frequency bandwidth can cause severe interferences between these services. The target PoC will consider MCC related scenarios to illustrate how the candidate waveform can support the very low latency requirement of MCC services. Furthermore, the coexistence (in the same bandwidth) aspects with more conventional services like Mobile BroadBand (MBB)
using different numerologies can be considered. The flexible platform illustrated in Figure 2-1 will be used for this scenario with appropriate GUI at the transmitter side to select the corresponding specific parameters (e.g. TTI). The GUI at the receiver side displays relevant KPIs in terms of latency and bit error rate (BER), in addition to the KPIs related to the implementation complexity.

For all targeted scenarios, most system parameters are selected from LTE for comparison purpose.

Using Telecom Bretagne’s PoC platform, several performance metrics can be evaluated such as:

- Power consumption (comparative measures using considered FPGA platforms, and accurate estimation for application-specific integrated circuit (ASIC) target technology)
- Hardware complexity (computational and memories)
- Power spectral density (compliance to a particular spectral mask, measure of out-of-band leakage)
- Channel impulse response (visualization for the current frame)
- Error-rate computation (plot of BER curves)
- Throughput evaluation (gross and net bitrate)
- Latency (number of clock cycles)
- Robustness against Doppler and synchronization errors

### 2.1.2 FBMC transceiver algorithm and control functionality

#### Advantages of FBMC/OQAM with respect to CP-OFDM

FBMC is a multichannel transmission scheme that introduces a filter-bank to enable efficient pulse shaping for the signal conveyed on each individual subcarrier. This additional element represents an array of band-pass filters that separate the input signal into multiple components or subcarriers, each one carrying a single frequency sub-band of the original signal. The process of decomposition performed by the filter bank is called analysis (meaning analysis of the signal in terms of its components in each sub-band); the output of analysis is referred to as a sub-band signal with as many sub-bands as there are filters in the filter bank. The reconstruction process is called synthesis, meaning reconstitution of a complete signal resulting from the filtering process. Such a transceiver structure usually requires a higher implementation complexity related not only to the filtering steps but also to the applied modifications to the modulator/demodulator architecture. However, the usage of digital polyphase filter bank structures [BD74][SSL02], together with the rapid growth of digital processing capabilities in recent years have made FBMC a practically feasible approach.

As a promising variant of filtered modulation schemes, FBMC/OQAM, originally proposed in [Sal67] and also called OFDM/OQAM [SSL02], can usually achieve a higher spectral efficiency than CP-OFDM since it does not require the insertion of a CP. Additional advantages include the robustness against highly variant fading channel conditions and imperfect synchronizations by selecting the appropriate prototype filter type and coefficients [LGS14].

4G/LTE is based on CP-OFDM multicarrier modulation. According to Balian-Low theorem [Bal81], CP-OFDM:

1) respects the complex orthogonality,
2) is poorly localized in frequency domain by adopting a rectangular waveform,
3) wastes part of the available bandwidth due to the addition of a CP.

The property in 2) results into a high Out-Of-Band Power Leakage (OOBPL) and large guard-bands have to be inserted to respect ACLR requirement. Furthermore, it results into a poor robustness against Doppler shift and spread. Further possible disadvantages of the
corresponding CP-OFDM system are related to flexible spectrum usage scenarios, where spectrum sharing and fragmented usage are not efficiently supported. To overcome the shortcomings 2) and 3) of CP-OFDM, FBMC/OQAM:

- a) relaxes to real field orthogonality,
- b) is better localized in the time-frequency plane, as defined by the Heisenberg parameter [DS10], depending on the used prototype filter,
- c) uses efficiently available bandwidth to achieve a higher spectral efficiency.

Property a) is obtained by changing the way QAM symbols are mapped onto each subcarrier. Instead of sending a complex symbol (I and Q) of duration T like in classical CP-OFDM, the real and imaginary parts are separated and sent with an offset of T/2 (hence the name Offset-QAM). Improvement b) comes from the introduction of the filter-bank and therefore highly depends on its type and coefficients. Property c) is the consequence of the absence of a CP. Previous published works have identified two major design criteria for an FBMC/OQAM system:

- Time Frequency Localization (TFL) criterion: for a better localized waveform in time and frequency domains thanks to the prototype filter. It is predictable that FBMC systems exhibit better robustness than CP-OFDM in doubly-dispersive channels and in the case of communications with synchronization errors. To this purpose, filter designs with the optimized TFL criterion have been proposed, such as Isotropic Orthogonal Transform Algorithm with overlapping factor (q) equals to 4 (IOTA4) [FAB95].
- Lower sideband criterion: for achieving low out-of-band power leakage in frequency domain and for improving spectrum coexistence with other systems. To this purpose, particular filter types should be used such as Martin-Mirabassi-Bellanger with q equals to 4 (MMB4) [LGS14][Mar98], considered for FBMC/OQAM during PHYDYAS project [PHYD].

FBMC/OQAM constitutes an enabler to several 5G services as it enhances system robustness to different types of impairments. For instance, the robustness of FBMC/OQAM against Doppler shift and spread can be exploited to support vehicular to anything (V2X) services. Furthermore, asynchronous communication can be envisaged with FBMC/OQAM thanks to its low OOBPL, enabling MMC services.

FBMC/OQAM system description and implementation

In the literature, typical implementation of FBMC/OQAM employs a PolyPhase Network (PPN) based structure [Hir81]. It is composed of one inverse fast Fourier transform (IFFT) followed by one PPN for the filtering stage, and enables a low complexity implementation of the FBMC/OQAM transceiver. To support the QAM scheme, the IFFT and the PPN must be duplicated, except at the transmitter side, thanks to the reduced complexity transmitter structure proposed in [NAB16].

If M is the total number of available sub-carriers, \( N_s \) the number of FBMC symbols in one radio frame and \( a_n(m) \) the Pulse-amplitude modulation (PAM) symbol at subcarrier index m and time slot n, then the baseband signal \( s(k) \) can be mathematically decomposed into the following equations:

\[
\begin{align*}
  s(k) &= s_0(k) + s_1(k) = k - \frac{M}{2}, \quad (1) \\
  s_1(k) &= \sum_{n=0}^{N_s-1} g(k - nM)u_{2n+i}(k), \quad (2) \\
  u_n(k) &= \sum_{n=0}^{M-1} a_n(m)\phi_n(m)e^{j\frac{2\pi km}{M}}, \quad (3)
\end{align*}
\]
with $j^2 = -1$. To keep the orthogonality in the real field, $\phi_n(m)$ must be a quadrature phase rotation term: $\phi_n(m) = j^{n+m}$. The impulse response of the prototype filter is $g$, with $g(i) = 0$ when $i \notin [0; L - 1]$, where $L$ is the length of the prototype filter ($L = qM$). Finally, equation (1) is decomposed between even ($2n$) and odd ($2n + 1$) FBMC time index symbols to represent the final overlapping sum due to OQAM processing.

Figure 2-2 illustrates all the required steps to compute the FBMC/OQAM baseband modulation signal using PPN implementation, and can be deduced from the previous equations:

1) $a_n(m)$ is obtained from a QAM mapper equivalent to CP-OFDM, with separation of real and imaginary parts respectively at time index $2n$ and $2n + 1$.

2) The pre-processing unit computes the phase term $\phi_n(m)$.

3) $u_n(k)$ in equation (3) represents the outputs of two IFFT blocks which process separately the real and imaginary sub-carriers.

4) Finally, equation (2) shows the PPN filter decomposition, and the final overlap and sum due to OQAM processing is described in equation (1).

It is possible to avoid the use of two IFFT blocks at the transmitter side through the use of pruned FFT algorithm. This leads to a reduced-complexity implementation presented in the work detailed in [NAB16] and [DS11]. When using a short filter ($q = 1$), this latter can be seen as a windowing operation: the outputs of the IFFT are simply multiplied by the prototype filter impulse response $g$. Consequently, the hardware complexity overhead introduced by the PPN is limited.
Receiver side implementation applies dual operations with respect to the ones performed by the constituent blocks of the transmitter. The IFFT must be replaced by an FFT, and all the operation order must be reversed: PPN, FFT then post-processing and OQAM demapper.

**Planned activities with respect to the current available FBMC/OQAM PoC**

This activity takes advantage of an available FBMC/OQAM PoC. The objective is to evaluate the impact of this waveform on other signal processing techniques such as synchronization, equalization, channel estimation, and MIMO. Typical SoTA techniques will be considered in addition to the investigation of novel algorithms and optimizations. Some of these techniques are detailed below, and others will be explored during the project.

The equalization procedure tends to be more difficult due to the absence of CP when the delay spread of the multipath channel is large. Thus, multi-taps equalizer seems to be required instead of the low-complexity one-tap equalizer as in CP-OFDM. However, the Frequency-Spread (FS) implementation of the FBMC/OQAM enables to correctly equalize multipath channel without increasing the complexity of the equalizer. The principle is to process the filtering stage in the frequency domain instead of the time domain for the PPN implementation. Thus, one-tap equalization can be achieved between the FFT and the filtering operation, and outperforms the PPN implementation when facing multipath channel [DBC+14]. Furthermore, the FS implementation also enables to greatly increase the robustness of FBMC/OQAM against timing errors due to imperfect synchronization up to 25% of the symbol duration for the case of MMB4 filter [DBC+14]. Therefore, one tap equalizer will be implemented and tested with FS implementation. A second known issue of the FBMC/OQAM modulation concerns the presence of a tail at the beginning and the end of a radio frame due to the filter convolution. Since 5G aims to use short frame sizes for several communication scenarios in order to reduce latency [5G-PPP], the resulting spectral efficiency losses can be non-negligible. However, the tail length is directly related to the length of the used prototype filter. Thus, a short filter like TFL1 (length $M$ samples) [PS13] only has a tail of length $M/2$ samples (due to the OQAM scheme), greatly reducing the spectral efficiency loss and the hardware complexity at the cost of a slightly higher OOBPL when compared with long prototype filters like MMB4 [DBC+14]. Both TFL1 and PHYDYAS filters will be implemented and compared in terms of spectral efficiency, hardware complexity and performance.

Finally, a principal challenge of the FBMC/OQAM modulation concerns the use of MIMO techniques, mainly in case of spatial diversity. Indeed, the FBMC/OQAM baseband signal is not segmented in independent blocks as in CP-OFDM due to its overlapping nature. Thus, applying Alamouti scheme to FBMC/OQAM results in unavoidable intrinsic interference [LSL10]. It is however possible to group the OQAM symbols in a pseudo-block structure to avoid interferences as proposed in [RIS10]. There is however two issues with this solution. First, it increases the memory requirement of the transceiver, since all the samples in a frame have to be stored. Second, this solution introduces a spectral efficiency loss. However, the memory overhead is reduced in the case of short frame size, and the spectral efficiency loss is also reduced in case of short prototype filters. Fortunately, this intrinsic interference is avoidable in the case of spatial multiplexing. However, maximum likelihood (ML) detection complexity may represent a main challenge for a hardware design in this case.

### 2.1.3 FC-OFDM transceiver algorithm and control functionality

**Motivation for using a flexible waveform in 5G**

In cellular communication systems, the most advanced technology, i.e. LTE/LTE-A, adopts the CP-OFDM as its physical layer modulation scheme, which has proven to be very efficient for the Mobile BroadBand (MBB) service. One particularity of 5G is the multi-service environment. Besides the traditional MBB service, 5G cellular systems expect to offer other
emerging services such as MMC and V2X. Although CP-OFDM is already well optimized for MBB, its application in other service scenarios is still questionable and far from optimum.

As an alternative solution to CP-OFDM, FBMC/OQAM has been seriously investigated in MMC and V2X scenarios due to its ability of supporting high mobility and relaxing synchronization constraint. According to the METIS project conclusions [METIS-D65], the FBMC/OQAM modulation is indeed advantageous and suitable for the machine type applications. However, FBMC/OQAM is not fully compatible with OFDM-based solutions such as MIMO and pilot design, so that the LTE pilots and MIMO design cannot be straightforwardly reused in the FBMC/OQAM-based systems. It is a serious challenge for the FBMC/OQAM scheme, since the best effort MBB, which seeks for more throughput with advanced MIMO solutions [IDM+11][RPL+13], will continue playing a major role in future 5G systems. Therefore, it is naturally preferred that any potential 5G waveform candidate shall prove that, besides its advantages, its usage will not create severe negative impact on the MBB service.

Motivated by the above facts, alternative solutions have to be considered. In a multi-service environment, it can be difficult to find a one-fits-all scheme. Moreover, an ideal modulation scheme should be flexibly adaptable when the requested service changes. For this purpose, the proposed FC-OFDM solution [Lin15] aims to enable a sub-band-based flexible configuration depending on the requested services. It can configure the filter coefficients as well as the signaling mode for the multi-service adaptation. Therefore, its high degree of waveform flexibility can bring superior performance than fixed waveform schemes such as CP-OFDM or FBMC/OQAM.

**FC-OFDM system description and implementation**

The idea of FC-OFDM is to allow the base-station to independently configure the waveform characteristic within each sub-band (Resource Block in 4G/LTE) according to the allocated service. Thus, each sub-band can be configured with 4G/LTE based waveform for MBB type services or with filtered waveform for emergent 5G services as V2X or MMC. For this purpose, three configuration modes, which can coexist within the same bandwidth, are proposed for the downlink transmission:

- Configuration mode 1 corresponds to a classical CP-OFDM modulation with insertion of a CP. Thus, it is fully compatible with MBB services currently provided in 4G/LTE standard. In addition, a postfix and a windowing operation is added to reduce the OOBPL.
- Configuration mode 2 can be seen as an FBMC/OQAM modulation using a half-sine shaped filter with overlapping factor equal to 1. The major difference is the introduction of post-processing stage after the IFFT which inserts a prefix, a postfix and a windowing operation. This mode conserves some advantages of FBMC/OQAM described in the previous sub-section. For instance, it can be used to improve the robustness against Doppler shift/spread in case of high mobility for V2X services, or for MMC services due to its capability to support asynchronous communication.
- Configuration mode 3 uses the same modulation and processing technique as described for mode 2, but at half data rate. Only PAM symbols are sent through the channel instead of OQAM symbols. The principal advantage of this mode is its orthogonality to both mode 1 and mode 2. Thus, instead of inserting a guard band (composed of null subcarriers), FC-OFDM with configuration mode 3 can be used between two sub-bands respectively configured in mode 1 and 2 to avoid important loss in spectral efficiency [Lin15].

Table 2-1 summarizes the properties of these three configuration modes.
### Table 2-1: Characteristics of the three FC-OFDM configuration modes.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Filter shape</th>
<th>Coefficients</th>
<th>Even symbol index</th>
<th>Odd symbol index</th>
<th>Orthogonality</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Rectangular</td>
<td>[1]</td>
<td>QAM</td>
<td>0</td>
<td>Complex, with mode 1 and 3</td>
</tr>
<tr>
<td>2</td>
<td>Half-sine</td>
<td>[1, -1]</td>
<td>PAM</td>
<td>PAM</td>
<td>Real, with mode 2 and 3</td>
</tr>
<tr>
<td>3</td>
<td>Half-sine</td>
<td>[1, -1]</td>
<td>PAM</td>
<td>0</td>
<td>Real, with mode 1, 2 and 3</td>
</tr>
</tbody>
</table>

The implementation of the FC-OFDM modulator is based on two IFFTs, as shown Figure 2-3. First, a QAM mapper is used for mode 1, and a PAM mapper followed by a quadrature phase rotator is used for mode 2 and 3. Then, for these two last modes, a filtering operation is realized in frequency domain. It consists of a trivial convolution with coefficients [1, -1], which corresponds to a half-sine shape in time domain. The advantage of using a frequency representation is that only one IFFT is to be used to compute the 3 modes at the same time (instead of 3 IFFTs), since each mode generates a set of sub-carriers which can be mapped directly to the IFFT. However, to support mode 2, a second IFFT must be used to generate the staggered path due to the OQAM processing, at odd symbol index.

The post-IFFT processing in Figure 2-3 contains two steps. In the first step, a prefix and a postfix are appended to the time domain modulated symbol. As shown in Figure 2-4 the prefix not only includes a CP but also an interval devoted to windowing called Roll-off Interval (RI); while the postfix only includes RI. Moreover, post-IFFT processing for handling the prefix and postfix at even symbol index is different from that at odd symbol index corresponding to the staggered path for OQAM processing. As it can be seen from Figure 2-4, at even symbol index, the prefix is a duplicate of the last \( L_{CP} + L_{RI} \) samples of the modulated symbol, where \( L_{CP} \) and \( L_{RI} \) are the intervals of the CP and RI in samples. Then the postfix, copied from the first \( L_{RI} \) samples of the modulated symbol, is appended at the end. Concerning the odd symbol index case, the modulated symbol is first evenly cut into two portions. Then, the prefix is added to the beginning of the second half portion; while the postfix is appended to the end of the first half portion. In the second step, a windowing operation is applied on the RI samples, for instance with a raised cosine window as the window function.
Concerning receiver side, dual operations must be used to recover the QAM/PAM samples: remove CP, RI and window, FFT, filtering then quadrature phase rotation and extraction of the real part for mode 2 and 3.

Figure 2-3: FC-OFDM transmitter architecture based on 2 IFFT.

Figure 2-4: Post-IFFT processing at even and odd symbol index.
As in CP-OFDM modulation, FC-OFDM uses a CP and thus suffers from spectral efficiency losses. However, due to a better spectral confinement thanks to the attenuated secondary lobes, 10 RBs (120 sub-carriers) can be saved for a bandwidth of 20 MHz in 4G/LTE when compared to CP-OFDM, increasing the spectral efficiency by around 10% [Lin15]. Although the introduction of a protection band between mode 1 and mode 2 and the loss of 1 sub-carrier due to the filtering operation of mode 2 and 3, FC-OFDM can potentially achieve better spectral efficiency than CP-OFDM.

The FC-OFDM solution for uplink is naturally different from that of the downlink as it targets different use cases. The details of the FC-OFDM uplink solution are reported in [FAN16-D31].

2.1.4 UF-OFDM transceiver algorithm and control functionality

UF-OFDM is a promising 5G waveform candidate [WS15][FAN16-D31], close to CP-OFDM, but with improved spectral properties. A novel frequency domain generation method for UF-OFDM is proposed, where overlapping subbands are superimposed to bring down UF-OFDM multi-carrier modulator complexity almost as low as a factor of 2 above CP-OFDM, with a negligible approximation error. Only the reduced complexity UF-OFDM transmitter implementation as described hereafter will be considered for hardware implementation and joint PoC.

Baseline UF-OFDM complexity

In order to introduce the reduced complexity UF-OFDM modulator, we provide first a brief summary of the baseline frequency domain implementation. For upsampling, the data symbols in frequency domain require $B$ FFTs of size $N_{OS}N$ and $B$ IFFTs of size $N$, where $B$ represents the number of subbands, and $N_{OS}$ the upsampling factor applied to the modulator ($N_{OS} = 2$ for a good trade-off between complexity and performance [WS15]). For the frequency domain filtering $6BN_{OS}N$ real operations are needed. Summing up the subband contributions leads to $2(B-1)N_{OS}N$ real summations. Finally an IFFT of size $N_{OS}N$ is required. Thus the overall complexity can be expressed as follows:

$$c_{UF, full} = B [f_{FT}(N_{OS}N) + f_{FT}(N) + 6 N_{OS}N] + 2(B-1)N_{OS}N + f_{FT}(N_{OS}N)$$  \hspace{1cm} (4)

which is at least by factor $N_{OS}B$ higher than CP-OFDM. For LTE-like multi-carrier parameters with 15 kHz subcarrier spacing and a physical resource block (PRB) size of $n_i = 12, \forall i$, a 20 MHz bandwidth consists of $B = 100$ PRBs. So UF-OFDM in this exact “brute-force” frequency domain generation case, with full band transmission, would have more than 200 times the complexity of CP-OFDM. This is not desirable and thus an alternative solution has to be designed.

For comparison, the matrix-vector-operation-based time-domain baseline implementation, the “textbook approach”, for one subband requires:

$$c_{TD, 1PRB} = (BQ - 2)(N + L - 1)$$  \hspace{1cm} (5)

This has to be executed $B$ times. In a full band allocation it holds $B \cdot Q \approx N$. For $B \cdot c_{TD, 1PRB}$, using equation (5), the complexity order thus becomes $O(N^2)$.

Reduced UF-OFDM complexity

The idea for reducing the frequency domain implementation complexity exploits the fact that subband signals have to be generated with a lower sample rate, compared to the full band. Furthermore, the proposed technique cuts the signal in frequency and time to provide a low complex frequency domain signal approximation. The aim is to make the approximation error
negligible, e.g. much smaller than any distortions caused by the subsequent RF chain processing and digital RF preprocessing.

In the proposed reduced complexity UF-OFDM transmitter (Figure 2-5), $B$ small $N_{FFT}$-sized IFFTs have to be carried out, as well as $B$ small $N_{OS}N_{FFT}$-sized FFTs. The frequency domain filtering requires $N_{OS}N_{FFT}$ complex multiplications per subband.

All subband contributions have to be added up. Note that this does not account for the additions of known zero positions. Thus, the summation of $X_{total}$ is accounted for as adding $X_{filt}^{(i)}$ instead of $X_{full}^{(i)}$. Then a large $N_{OS}N$-IFFT is made. All these operations for UF-OFDM multicarrier modulation sum up into the following expression:

$$c_{UF, appr} = f_{FT}(N_{OS}N) + B [ f_{FT}(N_{FFT}) + f_{FT}(N_{OS}N_{FFT}) + 6 N_{OS}N_{FFT} ] + 2(B - 1) N_{OS} N_{IFFT}$$

(6)

The complexity order for UF-OFDM is thus $O\{ N \log N \}$, like CP-OFDM. The overall complexity is at least by factor $N_{OS}$ higher than CP-OFDM.

Further details about the reduced complexity transmitter for UF-OFDM can be found in reference [WS15]. In addition, the implementation of new improvements will be considered in this joint PoC in a second phase.

![Figure 2-5: Principle of UF-OFDM frequency domain signal approximation, illustrating generation of one subband $i$ with $N_{OS} = 2$.](image)

2.1.5 Platform description

Available hardware resources

The available proof-of-concept platform from Telecom Bretagne is suited for investigation of digital baseband algorithms and related hardware complexity (Figure 2-1). The digital processing is handled by the ZedBoard which integrates the recent Xilinx device: Zynq-7000 All Programmable SoC (System on Chip). This device, which belongs to the latest series 7
Xilinx programmable circuits, integrates a dual-core ARM Cortex-A9 processing system clocked at 677 MHz. The processing system integrates in addition several peripheral controllers for communication (including 2 instantiations of tri-mode gigabit Ethernet and USB2.0) and external memory management.

The platform can be programmed through two integrated interfaces: a USB-JTAG interface available through a Micro-B USB connector and a traditional Platform Cable JTAG connector. Once programmed, it runs typically in a standalone mode. Other executions modes (e.g. a hardware-in-the-loop system prototyping) can be built by the system designer using the on-board available communication interface (e.g. 10M/100M/1G Ethernet and USB 2.0). Furthermore, an embedded Linux kernel is included for running on the ARM dual-core Cortex-A9 with all required device drivers. This configuration opens interesting perspectives for a target demonstration where the software part is executed on-board rather than on a host computer.

This digital baseband platform is paired with off-the-shelf RF modules (Figure 2-1). Several boards are available with 1x1 or 2x2 RF capabilities (Analog Devices AD-FMCOMMS1/2-EBZ daughterboards). The RF interface is software-tunable across a wide range (70 MHz to 6 GHz) with varying channel bandwidth (200 KHz to 56 MHz). The board integrates 12-bit DACs and ADC. Regarding the software development aspect, full Linux support is provided by Analog Devices. Furthermore, a dedicated application-programming interface is available and can be used without an operating system to interact with the AD-FMCOMMS1/2-EBZ boards. The possibility to connect the AD-FMCOMMS1-EBZ RF board to high-capacity FPGA boards opens interesting perspectives on the demonstration of a wide range of compute-intensive FPGA-based radio applications.

**Development framework**

The different development steps, from algorithm specification to on-board validation and demonstration, are summarized in Figure 2-6.

The development framework entry consists of the description of the technical component to be demonstrated and the related aspects of usage scenarios and estimated performances. The description of the technical component includes the following: (i) a detailed description of the proposed algorithm/technique, (ii) a reference software model, including a reference software testbench, and (iii) supported system parameters, including those related to the target channel models.

The first step in the development framework starts by analyzing the selected technical component considering an implementation/demonstration perspective. The objective in this step is to achieve simplified algorithms which are suitable for hardware implementation. It also targets the exploration of inherent properties of the algorithm which can be exploited for low power implementations. In this context, quantization issues are studied in order to propose efficient numeric representation of the processed data algorithm. Impact of the proposed optimizations is assessed and compared against the MATLAB reference model and the target/estimated KPIs. Algorithm parallelization techniques are proposed and their efficiency is characterized. Furthermore, besides the computation complexity, communication and memory requirements (size and access rates) are analyzed in this step and optimization techniques are proposed. Results comparison considering the different proposed Post-OFDM transmission techniques and the reference CP-OFDM one are conducted at this step and at all the subsequent development steps.
The second step concerns the digital hardware architecture exploration. The objective is to exploit efficiently the proposed algorithm optimization techniques by selecting the most suitable hardware architectural choices in order to fulfill the target KPIs. Combination of algorithm/architecture optimization techniques are explored and proposed in this context with emphasis on parallelism techniques and architecture efficiency. The outcome of this step consists of an original architecture fully specified and ready for the hardware implementation step. The attainable performances are also fully characterized and compared to the reference ones from the MATLAB reference models. This step includes also the refinement of the reference software model (including the test-bench) into a bit-true model for validation and to be used as a reference for the hardware implementation.

The third step in the development framework concerns the hardware implementation using the adequate design methodologies and tools for the devised architecture. Besides the traditional digital hardware design approaches, the platform environment includes recent design methodologies and tools related to system-level design, high-level synthesis, application-specific instruction-set processor (ASIP) based design, multiprocessor architecture models, and network-on-chip design [MBM14]. The required design tools and expertise are available to evaluate and compare the implementation results at this level in terms of throughput, latency, area (complexity), energy consumption, and error rate performance. Validation and comparison with the reference software model are conducted at this level through behavioral and post-synthesis simulations.
The last step concerns the on-board implementation and the development of the final demonstrator environment. Typically, a complete communication system which integrates the considered technical component is developed and prototyped on the target FPGA-based platform. This includes optimized hardware architecture of the transmitter, the channel model, the receiver, a performance evaluation module, and a global controller.

### 2.2 FBMC-MIMO transceiver based on software programmable hardware

#### 2.2.1 Scenarios, use cases, system parameters and KPI

Flexible and efficient use of all available non-contiguous spectra for widely different network deployment scenarios is one challenge for the future 5G. To maximize spectral efficiency, the 5G air interface technologies will need to be flexible and capable of mapping various services to the best suitable combinations of frequency and radio resources. Therefore flexibility and good frequency localization of the waveform are key requirements.

The well localized frequency response of FBMC entitles the use of fragmented spectrum with minor interference on adjacent bands. Very good performances are also demonstrated in non-synchronous access (whatever the time delay between users) [FAN16-D31]. However, under the time-frequency localization relationship, the time localization is sacrificed, making FBMC difficult to adapt to short packet size. On the other hand, the absence of guard period gives FBMC an efficiency gain for larger packet size or broadcast transmission (in the DL for instance) [FAN16-D31].

As discussed in section 2.1.2, one of the challenges FBMC waveform is facing is the adaptation to multiple antenna schemes. MIMO decoding is indeed an open issue with FBMC/OQAM waveforms. Contrary to CP-OFDM, the complex orthogonality is broken and is used for multiplexing interference and data. In case of Alamouti scheme, perfect reconstruction of the signal is not possible due to the interference term. ML detectors are possible but the complexity of such detector brought by the self-interference generated by FBMC is not compatible with conventional receiver order of complexity. This issue is not straightforward and concepts have to be revisited, which is the main goal of this PoC.

The objective of this PoC is thus to combine an FBMC-based waveform with a 2x2 MIMO scheme, while conducting a trade-off analysis of complexity vs. impairments robustness vs. throughput. This PoC will allow evaluating the performance of the proposed scheme with a focus on relaxed synchronization and channel estimation in the multi-antenna case. As a consequence, the goals of the PoC are threefold: demonstrate that FBMC-based waveform is compatible with MIMO, show the impact of 5G waveform on legacy LTE (in a non-synchronous use case, where co-existence between the waveforms in adjacent bands is considered) and investigate the frame structure for FBMC.

The flexible 2x2 MIMO FBMC-like transceiver developed by CEA will be based on software programmable hardware including a large Zynq FPGA for baseband processing, an ARM dual core processor for the control and an off the shelf RF front-end.

The architecture of the transceiver is thus based around 3 main elements (see Figure 2-7):

- Large FPGA for intensive sample based computations (main PHY layer)
- Flexible embedded microprocessor (ARM) built around Linux OS for control
Agile RF Transceiver IC with ability to provide at least 2x2 MIMO. Using an agile RF component allows for flexible carrier frequency, with a support for current 4G bands from 700MHz to 2.6GHz.

Figure 2-7: overall architecture of the transceiver.

The target PoC environment is illustrated in Figure 2-8 where one board emulates a 5G base station (transmitter side) and a second board is used to emulate a 5G user equipment (receiver side). Both digital boards are extended by an RF interface to enable over-the-air transmission. The TX and RX of the waveforms will be implemented on the Zynq SoC (FPGA and ARM). The control and interface are ensured by the ARM cortex A9 processor embedded in the Zynq SoC and through the development of a dedicated Graphical User Interface (GUI). The GUI at the transmitter side is used to select mapping and modulation parameters like the quadrature amplitude modulation (QAM) constellation order, the Fast Fourier Transform (FFT) and the cyclic prefix (CP) sizes, the number of active subcarriers, etc. The GUI at the receiver side displays relevant performance metrics. The coexistence aspects with classical LTE waveform will be also considered as can be seen on Figure 2-8, in an HW in the loop approach meaning that the LTE/OFDM part will not be implemented in real HW. The MIMO channel will be an over-the-air channel that includes the TX and RX RF boards.

Figure 2-8: Envisaged scenario for MIMO FBMC PoC

The main system parameters are following the LTE 10 MHz baseline, meaning a resource block granularity of 180 kHz and a TTI granularity of 1 ms, where each radio is 10ms long. The maximum number of resource blocks is 52, leading to a useful bit rate of 58 Mbps (2x2 mode with spatial multiplexing, and 64-QAM 3/4 for the modulation and coding scheme). The scenario under consideration is thus related to MBB core service and 50Mbps everywhere use case.
The performance metrics related to this proof of concept are:
- Hardware complexity (computational and memories)
- Bit Error Rate (BER)/ Packet Error Rate (PER) estimation on over-the-air transmission
- Throughput evaluation
- Out-of-band leakage

As can be seen from section 2.1.2, there are complementarities between CEA’s PoC and Telecom Bretagne’s PoC on MIMO FBMC. Whereas Telecom Bretagne will investigate block-wise Alamouti using short prototype filter, CEA will focus on FBMC-based waveform combined with spatial multiplexing.

2.2.2 PHY and MAC layer transceiver algorithm and control functionality.

The proposed application will implement parts of a 5G downlink physical layer transmitter and receiver. To keep the complexity of this application at a reasonably level, only a subset of the LTE physical layer features defined for 3GPP-LTE compliant devices is implemented. The following section gives a detailed overview over the implemented PHY features.

The downlink transmitter and receiver include the implementations of the following channels:
- Primary Synchronization Channel (PSCH), built from a Zadoff-Chu sequence
- Secondary Synchronization Channel (SSCH), built from a Zadoff-Chu sequence
- Physical Broadcast Channel (PBCH): in our proposed application, it carries information about cell and the set of the active physical resource blocks available for allocation.
- Reference signals, based on distributed pilots (time/frequency)
- Physical Downlink control channel (PDCCH)
- Physical Downlink Shared Channel (PDSCH)

2.2.2.1 Architecture overview for the transmitter

The downlink transmitter will be implemented in the CEA-Leti platform. A simplified block diagram is depicted in Figure 2-9.
As shown in the simplified block diagram in Figure 2-9, the transmitter performs the following tasks:
- Physical Broadcast Channel (PBCH) encoding
- Physical Downlink Control Channel (PDCCH) encoding
- Physical Downlink Shared Channel (PDSCH) encoding
- Mapping to RE and antenna processing if needed
- Time domain conversion and filtering

An allocation with a granularity of 1 ms is possible for the UE. The dynamic configuration of the active RB within the cell can be managed every 10 ms.

### 2.2.2.2 Architecture overview for the receiver

The downlink receiver will be also implemented into the CEA-Leti’s HW/SW platform. As shown in the simplified block diagram in Figure 2-10, it performs the following tasks:
- Synchronization and carrier frequency-offset (CFO) compensation
- Frequency domain conversion and filtering
- Demapping of the resource elements to the different physical channels
- Channel estimation and interpolation
- Equalization and MIMO detection
- Physical Downlink Control Channel (PDCCH) decoding
- Physical Downlink Shared Channel (PDSCH) decoding
The downlink receiver receives the IQ samples in time domain from the RF. The digital Front End (DFE) performs the IQ impairments compensation, digital down conversion, frequency shift and the down conversion from the ADC sample rate to the minimal sampling frequency.

The first processing step in the downlink receiver is the synchronization. Coarse time domain synchronization is performed based on the statistical properties of the signal (auto-correlation). Then the primary and secondary synchronization signals are used for radio-frame synchronization. Carrier frequency-offset (CFO) compensation is also performed based on an estimation derived from the synchronization algorithms. When the receiver has two received antennas, the initial synchronization is done on the antenna port with the maximum received power. The primary synchronization signal is detected by a correlation on the sign of the received signal. Only a subset of positions is tested thanks to the previous coarse synchronization process. To avoid misdetection, a validation unit checks that the peak amplitude is higher than a given threshold. After multiple synchronization signals are detected consecutively the position of the start of the radio frame is calculated. This position is used to pass an entire time-aligned radio frame to the subsequent modules.

After the frequency domain transformation, physical downlink channels are decoded. First the PBCH channel is extracted as depicted in Figure 2-11. The PSCH and SSCH are used to perform channel estimation. Linear interpolation is used to compute the channel coefficients for each Resource Element (RE). Then each RE is equalized and QPSK demapping is performed with corresponding Log Likelihood Ratio (LLR) computation. Then the transport channel is decoded after de-interleaving, de-rate matching and Viterbi decoding. The CRC is checked and if no error is detected, BCH message is extracted to determine the set of active RBs available for allocation. If the CRC is not correct, a new synchronization process is asked.

![Figure 2-10: Simplified block diagram of the proposed DL Rx](image-url)
When the message carried by the PBCH is decoded, the active RBs are extracted for each antenna and the PDCCH channel is decoded to determine the UE allocations. After that reference signals are demodulated for each receive antenna. Channel coefficients at reference signal locations are estimated after amplitude and sign compensation. A fine CFO estimation is then performed and the Channel Impulse Response is computed. Based on this new information, a frequency interpolation is performed followed by a time interpolation. The time interpolation is limited to a linear interpolation on 1ms (this part could be enhanced in the future if needed). Channel coefficients for each resource elements are stored and fed to the next processing blocks.

Given the active REs and the corresponding channel coefficients, RE corresponding to PDCCH are equalized. When Space Frequency Block Code (SFBC) is used, a simple linear detection is performed (ZF). LLRs are then fed to the transport channel decoder. If the CRC is valid, the UEs allocation is extracted. If the control manager detects that a resource block is dedicated to the UE of interest, the MCS and active RBs are interpreted and the PDSCH decoder’ chains are configured and activated. PDSCH are decoded and payload bits are sent to next layer when the CRC is valid.

The algorithms related to the PHY layer and the FBMC-based waveform for this PoC are currently under specification within WP3 (T3.1 and T3.2), especially focusing on the following aspects that are MIMO scheme and FBMC adaptation, channel estimation and synchronization. Further details on these building blocks and associated algorithms will be given in future deliverables of WP3 and WP5.

### 2.2.3 Platform description

The CEA-Leti’s HW platform is composed of a main baseband board developed by CEA-Leti and an off-the-shelf radio frequency board named ARRADIO and developed by Terasic. These two boards are duplicated for Transmitter and Receiver parts. As a consequence, the equipment
is identical for both transmitter and receiver, only their programming is different between TX and RX sides.

### 2.2.3.1 Architecture of CEA-Leti’s main board

The baseband processing is performed on CEA-Leti’s boards whereas radio transmission is done using the AD9361 chips of ARRADIO Terasic board.

The main baseband board has a reduced size (110x75mm) but still with high computational capabilities. Indeed, its main component is a high end Zynq-045 Xilinx FPGA, which integrates a dual Cortex-A9 ARM microprocessor with many interfaces possibilities.

#### 2.2.3.1.1 Main components

As described in Figure 2-12, the main components of the baseband board are:

- 1 FPGA Xilinx Zynq XC7Z045-1FFG676C (350K Logic cells / 900 DSP (25x18 multiplier) / 545 Blocks RAM 36Kb)
- This Zynq SoC (system on chip) integrates also 1 dual ARM Cortex-A9 microprocessor with its peripherals: two 1000 Mbps ethernet MAC, 2 USB OTG, 2 SD controllers, 2 full duplex SPI ports, 2 high speed UART…
- 1 dual ADC AD9643-250 14 bits / 250 MHz
- 1 dual DAC AD9122 16 bits / 1230 Msps (with 3 interpolators, NCO and integrated digital mixer)
- 1 ethernet transceiver 88E1518 (ethernet 10/100/1000Mps)
- 1 microSD card (compact flash) for ARM and FPGA programming
- 1 Flash memory 512Mbits S25FL512
- 1 dual LNA/VGA AD8332
- External interfaces:
  - 1 Samtec QSH-090 connector for HSMC (high speed mezzanine card) daughter board plug-in. Digital HCMOS 1v8 and LVDS links directly connected to FPGA.
  - 2 Samtec QSE-020 connectors for other daughter board plug-in
  - 1 ethernet RJ45 connector
  - 4 SMA connectors for analog Tx/Rx signals.

#### 2.2.3.1.2 Functional block diagram

The main baseband processing is done in the Xilinx FPGA X7Z045. The ARM processor manages the MAC interfaces in Linux environment and also the interfaces with the external world.

The plug-in of different daughter board types is possible on CEA-Leti’s main board:

- Daughter boards with fully digital interfaces through HSMC connector. These daughter boards are plugged on the bottom side of the CEA-Leti’s main board through one QSH-090 Samtec connector.
- Daughter boards with analog signal interfaces. These daughter boards are plugged on the top side of the main CEA-Leti’s board through the two QSE-020 Samtec connectors.

At the transmitter side, the conversion from baseband signals to an intermediate frequency signal can be done inside the AD9122 DAC, which integrates interpolators and NCO modulation. At the receiver side, the dual conversion (IF to baseband) can be done in the FPGA. Additional HCMOS 3v3 lines are also available on these QSE connectors for the control of the daughter by the main board.
2.2.3.1.3 PCB and dimensions

The printed circuit board of CEA-Leti’s main board is 10 layers. The main component Zynq-045 is connected to the PLL, ADC, DAC and HSMC ARRADIO daughter board through LVDS links. The main board routing and PCB is depicted in Figure 2-13.

![Figure 2-13: CEA-Leti's main board routing and PCB.](image-url)
The size of CEA-Leti’s main board is reduced to 110x75mm (including the 27x27mm FPGA) whereas the size of ARRADIO board is 69x84mm (see Figure 2-14).

Both QSE-020 connectors (J7/J8) are on top side, whereas HSMC QSH-090 is on bottom side.

The two boards (main CEA-Leti and its daughter ARRADIO) can be inserted in a small 115x78x43 mm aluminum box (see Figure 2-15).

**2.2.3.2 HSMC daughter board**

Different HSMC (High speed mezzanine card) can be used with CEA-Leti’s board which is compatible with Altera HSMC specification. For the envisaged PoC, ARRADIO Terasic board will be used with CEA-Leti’s main board.

The main component of the ARRADIO board is the AD9361 from Analog Devices [AD9361]. The AD9361 is a high performance, highly integrated radio frequency (RF) Agile Transceiver which combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers.
The AD9361 operates in the 70 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported. The architecture of the component along with the description of both transmitter and receiver are given in Appendix.

![Image of AD9361 schematic](image)

**Figure 2-16:** ARRADIO board top and bottom views.

A picture of the CEA-Leti’s HW platform, integrating the main baseband board and the off-the-shelf ARRADIO Terasic board is given below, highlighting the small form factor of the platform.

![Image of CEA-Leti’s HW platform](image)

**Figure 2-17:** CEA-Leti’s HW platform, top and bottom views.
2.3 Pulse shaped OFDM for timing adjustment (TA)-free low latency transmission

For WP5, Huawei intends to develop a Hardware-In-the-Loop (HWIL) platform and evaluate the Pulse shaped Orthogonal Frequency Division Multiplexing (P-OFDM) designed in WP3.

2.3.1 Scenarios, use cases, system parameters and KPI

PoC activities at Huawei will be mainly focused on two scenarios, namely asynchronous transmission for MMC and high mobility scenario for V2X.

- **Asynchronous transmission based on P-OFDM waveform**

In classical CP-OFDM systems, uplink synchronization needs to be established before any data transmission. A UE sends random access preamble so that its timing can be estimated at the Base Station (BS). Then a timing advance message is conveyed from the BS to the UE. The UE adjusts its timing accordingly. This so-called random access procedure aims to guarantee that the frames transmitted from all UEs are aligned at the BS [36.300]. However, as the number of UEs increases, this procedure may cause significant signaling overhead to the network.

Unlike CP-OFDM system whose performance highly relies on the uplink synchronization, P-OFDM with subcarrier level filtering offers an additional degree of freedom to the system design. One example is that, a pulse shape which spreads multiple symbol periods in time provides certain robustness against timing misalignment. Such a property of the new waveform brings room for simplified access procedure design that enables low latency massive machine type communication.

In this scenario, we consider three UEs accessing the system bandwidth simultaneously. Each of the three UEs occupies a fraction of the available bandwidth, which means that the subbands from different users are orthogonal in the frequency dimension. No timing synchronization among the three UEs is acquired; therefore no Timing Adjustment (TA) procedure is performed.

Asynchronous multiple access is regarded as a prerequisite of TA-free and grant-free access. It is especially of interest for several use cases such as sensor networks, automatic traffic control/driving. For this scenario, LTE CP-OFDM is taken as baseline for comparison. The KPIs include reliability in terms of Packet Error Ratio (PER), and BER, as well as signaling overhead.

- **Single link real time evaluation in high-velocity scenario**

V2X scenario is of great importance for 5G use cases, e.g. high speed train and automatic traffic control/driving. Given pulse shape design as an additional degree of freedom, the system robustness against double dispersive channel can be tuned accordingly. For comparison, IEEE 802.11p is considered as baseline. The KPIs of interests includes reliability, mobility, complexity and latency aspects.

2.3.2 PHY and MAC layer transceiver algorithm and control functionality.

In WP3, Huawei’s waveform research focuses on P-OFDM. The goal is to support massive access for machine type communication and high mobility by exploiting the additional degree freedom of pulse shaping.

2.3.2.1 Pulse shape design

In general, a P-OFDM transmitted signal $s(t)$ can be defined as

$$s(t) = \sum_{n=-\infty}^{+\infty} \sum_{m=1}^{M} a_{m,n} g(t - nT) e^{j2\pi mFt},$$

(7)
where $a_{m,n}$ is the complex-valued data symbol. Here, $M$ denotes the number of subcarriers, $m$ is the subcarrier index, $n$ refers to the OFDM symbol index, $T$ is the symbol period while $F$ is the subcarrier spacing. The transmit pulse shape $g(t)$ is designed to be of length $L = KT$ with $K \geq 1$. The overlapping factor $K$ can be interpreted as the total pulse duration with respect to the number of symbol periods.

Based on this signal definition, CP-OFDM is simply a special case with a rectangular shaped pulse $g(t)$ of length $L = T + T_{CP}$. On the receiver side, the CP removal operation can be interpreted as a receive filter $\gamma(t)$ of length $L = T$. In our experiments, LTE specified CP-OFDM will be considered as baseline for performance evaluation.

For the P-OFDM design, as an initial step, symmetric design principle is adopted, namely matched filters are applied at the transmitter and the receiver sides in order to achieve maximum SNR, i.e. $g(t) = \gamma(t)$ [SB03, STR98, BOE99, JW07]. In order to support transmission with relatively large timing misalignment, an orthogonalized Gaussian pulse with the length constraint $K = 4$ is employed [ZSW15]. The designed pulse shape, as well as the corresponding pulse shape for CP-OFDM, is depicted in Figure 2-18.

![Figure 2-18: Pulse shapes considered.](image)

### 2.3.2.2 Transceiver structure

Thanks to the fact that uniformed pulse shaping filter is applied to all given subcarriers, P-OFDM transceiver can be efficiently implemented using a PolyPhase Network (PPN). Figure 2-19 provides a design example. In contrast to the typical CP-OFDM transceiver, the “add CP” after the IFFT block at the TX side and the “remove CP” before the FFT block at the RX side are replaced by the synthesis and the analysis PPN, respectively. All the other functional modules remain the same.

![Figure 2-19: Asynchronous transceiver based on P-OFDM.](image)

Since a single antenna is deployed at the TX as well as the RX side, orthogonal access is required, namely, the resource allocated to different users must not be overlapped. However, the experiment can be extended to the multi antenna case. With multiple antenna deployed at the RX side, the system allows multiple UEs to access the time-frequency resource simultaneously.
2.3.3 Platform description

Huawei’s HWIL platform consists of two major components, as shown in Figure 2-20. The radio frequency frontend Remote Radio Unit (RRU) is based on National Instrument USRP X310 which is a high performance, scalable, software defined radio platform. The hardware architecture combines two extended-bandwidth daughterboard slots covering DC – 6 GHz with up to 120 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA. The daughterboards SBX and UBX are adopted.

The baseband processing is carried out on x86 based computational platform. It supports flexible implementation of algorithms for the base band processing of the received I/Q samples. As mentioned above, HWIL enables fast and flexible adaption of the selected algorithms as well as optimisation of the processing. The I/Q samples are generated, respectively processed, on the host processor and exchanged via the high speed interface to the X310 based RRU. Live over the air transmission enables tests with different real radio channels, distances and antenna configurations.

**Figure 2-20: Hardware in the loop platform based on USRP.**

Such hardware platform is employed at each transmitter/receiver unit. A typical setup of 3 users and 1 BS is planned to perform the test as shown in Figure 2-21. On the receiver side, GUI will be implemented, demonstrating the KPIs of interests to compare the new approach with other solutions and the state of the art solutions e.g. CP-OFDM.
2.4 Post- and Parameterized-OFDM Waveforms for Low Latency Transmission

2.4.1 Scenarios, use cases, system parameters and KPI

HHI intends to implement novel waveform concepts using its broadband radio modules with support for 2 and up to 8 transceiver branches. The implementation is based on a flexible software-defined radio approach, which is combined with high-performance computing platforms based on latest FPGAs, DSPs, and general-purpose server CPUs.

The PoC will include implementations of different baseline waveform concepts based on 4G’s CP-OFDM, as well as FBMC and a modified filtered CP-OFDM waveforms. The target is to develop and implement waveforms which will be parameterized for specific scenarios and used for coexistence studies in dense networks. The coexistence studies will be detailed in Section Error! Reference source not found.. Here, we will describe the novel waveform concept as well as HHI’s SDR platform used for the real-time implementation.

The use case includes a standard LTE network as well as an embedded novel waveform developed in FANTASTIC-5G. The system parameters to be altered may include but are not limited to the chosen carrier frequency, channel bandwidth, subcarrier spacing, power spectral density, as well as occupied time, frequency and spatial resources. The KPIs to be evaluated comprise SINR and resulting data rates, interference power as in the ACLR, as well as carrier frequency offsets (CFO) statistics when comparing orthogonal and non-orthogonal waveforms.

Furthermore, HHI plans to evaluate a modified waveform for the MCC use case. Here, the focus is on low latency transmission under reliability constraints as defined by the machine-type communication use case in the factory automation scenario. The KPIs to be evaluated include latency percentiles, latency jitter, and reliability targets under given data rate demands.

2.4.2 PHY and MAC layer transceiver algorithm and control functionality.
The input required is mainly coming from the radio-frame design done in WP4. HHI is working closely in WP4 on the algorithm design for the proposed scenarios. WP5 targets the implementation of key waveforms for the coexistence use case as well as for the special requirements for MCC. Results of HWIL experiments with injected impairments (interference, mobility) will be analyzed. For the MCC use case, a real-time low delay data transmission based on a customized PHY-MAC design will be implemented and evaluated.

The modified CP-OFDM waveform to be implemented is based on LTE’s multicarrier OFDMA downlink waveform, see also [PMW+16] for an initial description. The parameter set is chosen to fulfill ultra-reliable low latency communication (URLLC) service requirements as specified in [NGMN][ITU-R]. The envisioned waveform has potential to fulfill design goals and decrease latency on the physical (PHY) and medium access layers (MAC) by a factor of 10 and more when compared to state-of-the-art LTE-Advanced systems. The key parameters addressed in the waveform design are a modified subcarrier spacing, which is scaled by a factor $k$, as well as an optimized symbol termination in combination with the shortening of the transmission time intervals (TTI). On the higher layers, an optimized resource mapper schedules small packets which are adapted to the TTI structure in order to leverage on the optimized frame structure.

The table below compares a standard 20 MHz LTE downlink configuration ($k = 1$) with the chosen system parameters of the latency optimized multi-carrier waveform ($k = 4$). Here, $\Delta f$ refers to the subcarrier spacing, $f_s$ to the sampling frequency. The scaling factor can be modified according to the particular transmission requirements. The FFT sizes and symbol mapping and demapping functions scale accordingly.

<table>
<thead>
<tr>
<th>$k$</th>
<th>$\Delta f$ [kHz]</th>
<th>$f_s$ [MHz]</th>
<th>FFT size</th>
<th># of subcarriers</th>
<th># of symbols in 1 ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>15</td>
<td>30.72</td>
<td>2048</td>
<td>1200</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>60</td>
<td>30.72</td>
<td>512</td>
<td>300</td>
<td>56</td>
</tr>
</tbody>
</table>

Table 2-2: Used CP-OFDM and modified CP-OFDM parameter sets for the URLLC use case.

### 2.4.3 Platform description

HHI will use its SDR platforms [WMP+15] to evaluate algorithms and concepts of FANTASTIC-5G. The hardware toolkit consists of radio-heads in different configurations, DSP signal processing cards, as well as the MicroTCA chassis with management controller and backplane, see also Figure 2-22. All hardware cards are based on the MicroTCA form factor (single modules / full-size, 73.8x28.95x181.5mm) and interconnected via backplane and high-speed frontpanel connectors. MicroTCA is an open modular computing standard specified by PICMG. The MicroTCA chassis provides adequate power supply and cooling, high-speed connection via the backplane, as well as central control and management over the MicroTCA carrier hub. This allows a very flexible combination of modules depending on the requirements of specific use cases and scenarios.

The key hardware component is the radio-head, which uses the well-known AD9361 transceiver chip described in the appendix. The radio-head is available in a configuration with two transceivers for standard LTE / LTE-A signal processing. An advanced version of the radio-head (8TRx) uses up to 8 parallel transceiver chains, which are fully synchronized and are decoupled into 8 in- and 8 output channels. The 8TRx radio-head consists of an analog board based on several AD9361 as well as a digital board containing a Xilinx Zynq SoC (with embedded ARM Cortex-A9 processors). The AD9361 is a fully software-configurable, agile, 2 antenna 12-bit transceiver chip. It is tunable from 70 MHz up to 6 GHz, supports up to 56 MHz analog bandwidth and implements various transmission modes and filters.

Both radio-heads implement high-speed SFP connectors, which are located on the frontpanel. The 8TRx radio module has a QSFP port with support for up to 4x10 Gb channels. In addition,
both cards have a GbE frontpanel connector for standalone configuration as well as in- and output clock connectors for synchronization of several radio frontends. The backplane connectors provide configuration and management interfaces via a central MicroTCA management controller as well as the 12 V power supply. The digital high-speed ports operate GbE, CPRI 4.1 and 6.1 as well as 10 GbE on the Xilinx Zynq SoC. The implementation of the 10 GbE protocol is a full VHDL-core within the Xilinx Zynq FPGA, which also contains a full TCP/IP stack in VHDL. This can be connected to a standard 10 GbE server card for real-time data streaming from a GPP server.

Real-time signal processing can be implemented directly on the radio-head on the Xilinx Zynq FPGA, on a separate Texas Instruments DSP card, or on a third party Intel GPP. The MicroTCA TI DSP card has 4 SFP connectors and also implements GbE and CPRI 4.1. The DSP silicon is based on a dual TI C66x DSP (TMS320C6670), which contains various co-processors for FFTs, Turbo encoding, Viterbi decoding, bit-rate and network co-processors. The DSP is a multi-core processor containing 4 C66x cores, which support fixed- and floating-point operations at 1-1.2 GHz clock speed. All cores are interconnected via a high-speed memory bus. Both C66x SoCs are interconnected via a TeraNet high-speed bus supporting a 40-50 Gbps high-speed interconnection for joint signal processing.

The DSP firmware is a basic LTE compliant transmitter and receiver chain. The proprietary signal processing software implements basic MIMO-OFDM transmission, including real-time synchronization and equalization for over-the-air transmission in software. In addition, radio-head and DSP cards include Matlab interfaces allowing in- and output of data with an easy-to-configure interface from a standard PC. This allows non-real-time input of various waveforms and offline recording of received samples for HWIL experiments. The Matlab format is a simple 12-bit I/Q format, which can be provided to other partners for joint experiments.

Figure 2-22 HHI’s SDR toolkit based on MicroTCA form factor: The key components are radio-heads with support for 2-8 transceiver chains.
3 Coexistence aspects evaluation PoC

3.1 Scenario, use case, system parameters and KPI

HHI intends to extend the waveform studies and focus on coexistence aspects. The main purpose of the coexistence study is the evaluation of signal leakage of neighboring carriers and the resulting inter-carrier interference between legacy and new waveforms described in Section 2.4.2. This is done for legacy LTE waveforms, FBMC, as well as the latency optimized CP-OFDM waveform. The latency optimized CP-OFDM is mainly achieved by modifying subcarrier spacing and data mapping.

This previous waveform scenario will be extended to an interference-limited scenario with a dense reuse of spectral resources. Therefore, we will embed novel waveforms into legacy waveforms as well as add interference from external sources. For this, HHI has a standard LTE Rel. 9 network available, which provides a basic LTE coverage in LTE FDD and TDD bands. The novel waveform transmitter and receiver will be implemented to enable the combined signal analysis on the previously described SDR platform in Section 2.4.3.

The main KPIs to be evaluated are SNR, SINR, peak to average power ratio (PAPR), and ACLR.

In order to conduct coexistence studies with arbitrary waveforms, a generic multi-carrier modulator is integrated supporting various waveforms. Figure 3-1 shows the general transmission using multi-carrier (MC)-modulation.

For OFDM, the MC-modulation consists of a FFT. CP is added and the symbols are serialized before the conversion to the RF. The implementation of FBMC de-/modulator is based on the PHYDYAS framework [Bel08][PHYD], where an efficient implementation based on poly-phase networks is proposed. The Rx/Tx modules are implemented using MATLAB. In Figure 3-2, the integration of the MC modules in the HWIL setup is depicted schematically.

A MATLAB-based GUI can be used to control and parametrize the measurements. The parameters to be changed include the number of subcarriers, channel impairments, selected waveform, etc. Subsequently, the data-frames are generated with 307200 I/Q samples per frame which corresponds to 10ms at 30.72 MHz sample rate. A resolution of 12 bit is used. The data

![Diagram of multi-carrier transmission chain](image-url)
frame is sent to the SDR device using GbE and internal RF processing modulates the signal to the selected carrier frequency. The radio-frames are cyclically looped to simulate a continuous transmission. The Rx unit records pre-defined number of samples between 10..50ms at 30.72MHz. The recorded IQ samples are sent to PC using GbE and an offline synchronization based on Zadoff-Chu sequences is performed.

The basic HWIL signal processing chain is shown in the schematic below.
Figure 3-2 Integration of multicarrier modulator into HWIL testbed
Considering the signal for each device (as depicted in Table 3-1), the following parameters can be configured.

**Table 3-1: Parameters for multi-carrier modulator**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subcarrier</td>
<td>$N_{\text{subc}}$</td>
<td>16/32/64/128/256 …</td>
</tr>
<tr>
<td>Subbands</td>
<td>$B$</td>
<td>$1 \ldots N$</td>
</tr>
<tr>
<td>Subcarrier per sub-band</td>
<td>$n_i = N/B$</td>
<td>$1 \ldots N$</td>
</tr>
<tr>
<td>Filter length</td>
<td>$N_{\text{filter}}$</td>
<td>$&lt; &lt; N_{\text{subc}}$</td>
</tr>
<tr>
<td>Cyclic Prefix</td>
<td>$\text{CP}$</td>
<td>$1/7 \times N$</td>
</tr>
<tr>
<td>Overlap factor</td>
<td>$K$</td>
<td>$1/2/4/ \ldots$</td>
</tr>
<tr>
<td>Number of Symbols</td>
<td>$N_{\text{symb}}$</td>
<td>$1 \ldots 140$</td>
</tr>
</tbody>
</table>

### 3.2 PHY and MAC layer transceiver algorithm and control functionality.

The input required is mainly coming from the radio-frame design done in WP4. HHI is taking the waveforms and putting I/Q samples into the pre-defined I/Q streaming format. WP5 targets the implementation of key waveforms for the coexistence scenarios. Results of HWIL experiments with injected impairments (interference, high Doppler) will be transmitted over real channels as well as pre-defined channels with injected impairments. Results will be recorded for further offline analysis.

### 3.3 Platform description

In addition to the SDR platform presented in section 2.4.3, the combined signals will be analyzed using HHI’s Matlab toolchain, as well as a Rohde&Schwarz Signal analyzer (FSW). Both systems allow recording and offline processing of recorded measurement data.

The key components of HHI’s SDR toolkit to be used are the flexible radio-head with many high-speed interfaces to external processing units as well as the powerful TI DSP SoCs all interconnected using the MicroTCA standard. Results can be analyzed with HHI’s MATLAB toolchain as well as the Rohde&Schwarz FSW which has a basic signal analysis suite for evaluating signal power as well as the LTE option for analyzing LTE-based radio-frames. This can be used as reference when comparing novel waveforms to existing ones. The hardware toolchain consisting of several SDR toolkits and a Rohde&Schwarz analyzer as well as a MATLAB-based signal analysis GUI is depicted in Figure 3-3 below.
Figure 3-3 Coexistence Evaluation with HHI's SDR Toolkit
4 Broadcast and multicast SDR-based PoC

4.1 Scenario, use case, system parameters and KPI

Joint broadcast and multicast scenarios provide a higher degree of flexibility, especially in terms of QoS. On one hand, when the same content is shared by several users, broadcast services can reduce drastically the load of the network. However, it does not support reconfiguration or flexibility since it is constrained by the weakest user. On the other hand, MIMO techniques have provided a wide range of capabilities to enhance communication systems.

The aim of the proposed SDR PoC is to enable multicast transmissions to different multicast groups by the use of MIMO techniques but, at the same time, provide a common broadcast layer to all users. Hence, different levels of streams are multiplexed, depending if they are intended for multicast groups or for all users.

In LTE-A, there is no MIMO scheme applied in the broadcast transmissions of Multimedia Broadcast Multicast Service (MBMS) frames. Moreover, no multicast transmissions are supported by any mode of LTE-A. The proposed SDR PoC aims to provide this support and introduce the necessary tools to convey broadcast and multicast streams jointly at the same time.

In WP4, CTTC studies different scenarios with and without feedback considering broadcast and multicast transmissions jointly with an arbitrary number of users [FAN16-D41]. This research is studied and reproduced at small scale with two groups of multicast, with three receivers and one transmitter. Synchronization, channel estimation and equalization algorithms are up to CTTC implementation. Nevertheless, some enhancements provided by WP3 could be considered [FAN16-D31].

To reproduce the targeted scenario at small scale, two multicast groups are defined, which are spatially separated. The goal is to transmit 3 streams: one common to both groups and the rest as separated streams to each group. The first group will be integrated by a single receiver and the second group by two receivers. Figure 4-1 illustrates the proposed scenario.
As can be seen in Figure 4-1, broadcast stream is depicted in the blue line, and the multicast streams are depicted in red for the first multicast group, and in green for the second multicast group, respectively. Hence, we can guarantee that all members of the first group will receive red and blue streams, whereas the second group will receive green and blue streams. Although the blue stream is received by all members, the red and green streams are received depending on the group where the members are.

To replicate the proposed scenario, 4 USRP X300 are going to be employed, one configured as transmitter and the remaining as receivers. All USRP support two-antenna configuration. Figure 4-2 illustrates the proposed scenario using USRP nodes.

Following KPIs are taken under consideration:
- User data rate, in average terms.
- Throughput.
- Coverage, in terms of outage capacity.
- Complexity reduction as a secondary KPI.
4.2 PHY and MAC layer transceiver algorithm and control functionality

The PHY and MAC layer transceiver algorithm and control functionality are developed in WP4 [FAN16-D41]. CTTC is working closely in WP4 and is in charge of designing and providing the algorithms for the proposed scenario. In more detail, WP4 specifies 2 modes of multicast transmissions: by superposing codewords and by superposing beam patterns. In WP5, the second approach is proposed to be implemented, studied and analyzed. With the transmitter USRP, multicast beams and the broadcast beam are going to be superposed.

Moreover, in WP5, a scenario without feedback is considered, where the multicast groups are spatially distributed and the transmitter employs a fixed precoder along the transmission. Additionally, the receivers are static and do not present any mobility effects.

4.3 Platform description

To implement the proposed scenario, we use USRP X300 nodes, with the following specifications:

- Two wide-bandwidth RF daughterboard slots
  - Up to 120MHz bandwidth each
  - Daughterboard selection covers DC to 6 GHz
- Multiple high-speed interfaces
  - Dual 10 Gigabit Ethernet - 200 MS/s Full Duplex
  - PCIe Express (Desktop) - 200 MS/s Full Duplex
  - ExpressCard (Laptop) - 50 MS/s Full Duplex
Dual 1 Gigabit Ethernet - 25 MS/s Full Duplex

Table 4-1: USRP X300 specifications.

<table>
<thead>
<tr>
<th>Conversion Performance and Clocks</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Sample Rate (max)</td>
<td>200</td>
<td>MS/s</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>14</td>
<td>bits</td>
</tr>
<tr>
<td>DAC Sample Rate (max)</td>
<td>800</td>
<td>MS/s</td>
</tr>
<tr>
<td>DAC Resolution</td>
<td>16</td>
<td>bits</td>
</tr>
<tr>
<td>Host Sample Rate (16b)</td>
<td>200</td>
<td>MS/s</td>
</tr>
<tr>
<td>Internal Reference Accuracy</td>
<td>2.5</td>
<td>ppm</td>
</tr>
<tr>
<td>Accuracy w/GPSDO Option (not locked to GPS)</td>
<td>20</td>
<td>ppb</td>
</tr>
</tbody>
</table>

Figure 4-3: Front and back views of USRP X300.

The Table 4-1 describes the main specifications of USRP X300. Figure 4- illustrates front and back views of USRP X300.

To run USRP X300, we use the Cloud Architecture for Standardization Development (CASTLE), developed at CTTC. CASTLE features are described as follows:

- Hardware & Software multiplatform architecture (Windows, Linux and Mac OSX).
- It is a tool which implements different standards: LTE-A Rel.12, broadband global access network (BGAN), visible light communications (VLC).
- All PHY algorithms of LTE and BGAN.
- Remote management and interaction.
- Supports MIMO in LTE and BGAN via simulation or emulation.
- Includes non-standard defined procedures (channel decoding, synchronization, channel estimation, etc.)
- Written in C++.
- Web interface for simulations and scenario managing (HTML5, JavaScript, CSS3).
- Open API to manage the remote connections, in C++ and MATLAB.
- Allows to debug any intermediate signal processing block to embed own algorithms.
- Easy scenario configuration.
- Opened interface to upper layers. Primitives to be called by MAC layer.
- Flexible modification of standards’ parameters.
- Easy reconfiguration and on-fly reconfiguration.
5 Conclusions

This deliverable provided an overview of the planned PoC’s in FANTASTIC-5G. Three main categories of the demonstrations are planned: post-OFDM waveform prototyping, coexistence aspects evaluation and broadcast and multicast SDR-based PoC.

For each PoC, a description about the approved scenarios is provided by specifying the targeted use-case and the considered KPIs. Additionally, the selected techniques that will be adopted by each PoC are specified and the relation of the PoC to the different project WPs is determined. Moreover, the platforms that will be developed or used for each PoC are described along with the necessary PHY and MAC layer transceiver algorithms and control functionalities.

The post-OFDM waveform prototyping includes the development of FBMC-OQAM, FC-OFDM, UF-OFDM, and 2x2 MIMO-FBMC based transceivers. The first three transceivers will be implemented considering V2X, MMC and MCC scenarios while the 2x2 MIMO-FBMC will be tested in scenarios related to MBB core service. In addition to the mentioned transceivers, the post-OFDM prototyping includes the demonstration of P-OFDM in both asynchronous uplink transmissions in MMC and high mobility vehicular communication scenarios. The future effort within this category will focus on enriching the available platforms to support the identified scenarios, perform more components analysis and architecture exploration and realize the components validation step.

The coexistence evaluation targets the SINR, data rates, ACLR, and CFO evaluation in dense environment for different waveforms evaluations like LTE waveform, modified FBMC and latency optimized CP-OFDM. MCC scenario will be considered for the evaluation. The future efforts will focus on synchronization part in addition to the enhancement of the coding part.

The work on broadcast and multicast transmission will be demonstrated using SDR platforms. The demonstration will include the MIMO settings and the corresponding work on synchronization, channel estimation and equalization. The future work on this PoC includes the implementation of the corresponding frame and the validation of the synchronization and decoding in a single downlink shared channel and generate preliminary computational complexity profile.

The output of this deliverable will serve a reference to guide the preparation towards the implementation of the different components.
6 References


Appendix A

A.1 AD9361 architecture

The AD9361 integrates a dual transmitter and a dual receiver with 2 ADC 12bits and 2 DAC 12 bits.

Each receive (RX) subsystem includes independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9361 also has flexible manual gain modes that can be externally controlled. Two high dynamic range ADCs per channel digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best in class TX EVM of $\leq-40$ dB, allowing significant system margin for the external power amplifier (PA) selection. The onboard transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All (Voltage Control Oscillator) and loop filter components are integrated.

![Figure A-1: AD9361 architecture.](image)
### A.2 AD9361 Transmitter

The transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer.

The digital data received from the base-band board passes through a fully programmable 128-tap FIR filter with interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for upconversion.

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. At this point, the I and Q signals are recombined and modulated on the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional band shaping, and then the signal is transmitted to the output amplifier. Each transmit channel provides a wide attenuation adjustment range with fine granularity to optimize signal-to-noise ratio (SNR).

Self-calibration circuitry is built into each transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back through an unused receiver channel to the base-band board for signal monitoring. The TX monitor blocks are available only in time division duplexing TDD mode operation while the receiver is idle.

### A.3 AD9361 Receiver

The receiver section contains two independently controlled channels that can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer.

Each channel has three inputs that can be multiplexed to the signal chain, making the AD9361 suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a low noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that down convert received signals to baseband for digitization.

Gain control can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP (baseband processor) to make the gain adjustments as needed.

The receivers include 12-bit, sigma-delta (Σ-Δ) ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.